

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Rajski et al.

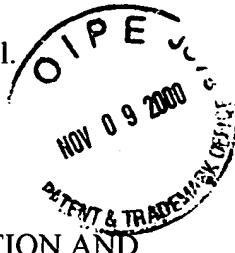
Application No. 09/620,021

Filed: July 20, 2000

For: CONTINUOUS APPLICATION AND
DECOMPRESSION OF TEST PATTERNS TO A
CIRCUIT-UNDER-TEST

Examiner: Not yet assigned

Date: November 6, 2000



Art Unit: Not yet assigned

CERTIFICATE OF MAILING

I hereby certify that this paper and the documents referred to as being attached or enclosed herewith are being deposited with the United States Postal Service on November 6, 2000 as First Class Mail in an envelope addressed to: COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.

Attorney for Applicant

3 / Prel. Amdt.

A
E. Willis
4-4-01TO THE COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231PRELIMINARY AMENDMENT

Prior to examination, please amend the application as follows:

In the specification:

Replace the paragraph at page 14, lines 20-27 with the following:

A1 Fig. 12 is a block diagram of a tester 21 embodiment that includes the decompressor 36, rather than providing it in the circuit 34. The tester decompresses the test pattern internally and transmits the decompressed test pattern to the CUT 24. Such a tester has advantages where testing time is not as critical and it is preferred not to add a decompressor to each circuit-under-test. Storage requirements are still reduced because compressed test patterns (rather than full test patterns) need only be stored. In addition, in a variation of the above tester embodiment, the compactors 38 can also be included in the tester 21 rather than the circuit 34. The circuit then returns uncompressed test responses to the tester. This further simplifies the circuit's design.

Replace the paragraph at page 12, lines 18-21 with the following:

A2 The variable x denotes a "don't care" condition. Then a corresponding compressed test pattern can be determined by solving the following system of ten equations from Fig. 7 using any